

# TLP2200

- Isolated Buss Driver
- High Speed Line Receiver
- Microprocessor System Interfaces
- MOS FET Gate Driver
- Direct Replacement For HCPL-2200

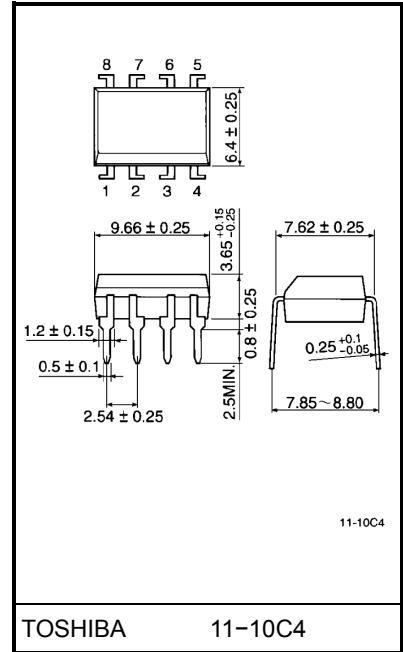
The TOSHIBA TLP2200 consists of a GaAsIred light emitting diode and integrated high gain, high speed photodetector. This unit is 8-lead DIP package. The detector has a three state output stage that eliminates the need for pull-up resistor, and built-in schmitt trigger. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1000V /  $\mu$ s.

- Input current:  $I_F = 1.6\text{mA}$
- Power supply voltage:  $V_{CC} = 4.5\sim 20\text{V}$
- Switching speed: 2.5MBd guaranteed
- Common mode transient immunity:  $\pm 1000\text{V} / \mu\text{s}$  (min.)
- Guaranteed performance over temp:  $0\sim 85^\circ\text{C}$
- Isolation voltage: 2500Vrms(min.)
- UL recognized: UL1577, file No. E67349

### Truth Table (positive logic)

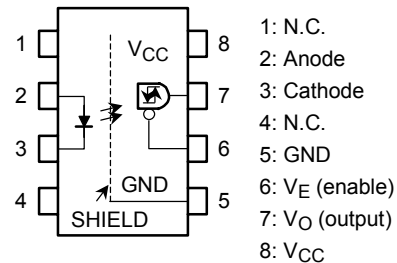
Input	Enable	Output
H	H	Z
L	H	Z
H	L	H
L	L	L

Unit in mm

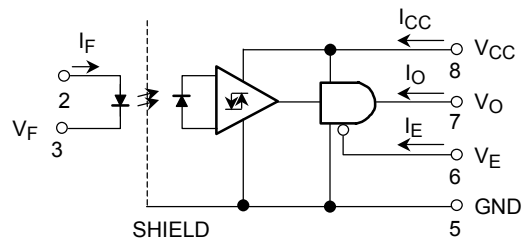


Weight: 0.54 g

### Pin Configuration (top view)



### Schematic



## Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input current, on	$I_{F(ON)}$	1.6	—	5	mA
Input current, off	$I_{F(OFF)}$	0	—	0.1	mA
Supply voltage	$V_{CC}$	4.5	—	20	V
Enable voltage high	$V_{EH}$	2.0	—	20	V
Enable voltage low	$V_{EL}$	0	—	0.8	V
Fan out (TTL load)	N	—	—	4	—
Operating temperature	$T_{opr}$	0	—	85	°C

## Absolute Maximum Ratings (no derating required up to 70°C)

Characteristic	Symbol	Rating	Unit
Forward current	$I_F$	10	mA
Peak transient forward current (Note 1)	$I_{FPT}$	1	A
Reverse voltage	$V_R$	5	V
Output current	$I_O$	25	mA
Supply voltage	$V_{CC}$	-0.5~20	V
Output voltage	$V_O$	-0.5~20	V
Three state enable voltage	$V_E$	-0.5~20	V
Total package power dissipation (Note 2)	$P_T$	210	mW
Operating temperature range	$T_{opr}$	-40~85	°C
Storage temperature range	$T_{stg}$	-55~125	°C
Lead solder temperature (10s) (**)	$T_{sol}$	260	°C
Isolation voltage (AC 1min., R.H. ≤ 60%, $T_a = 25^\circ\text{C}$ ) (Note 3)	$BV_S$	2500	Vrms

(Note 1) Pulse width 1μs 300pps.

(Note 2) Derate 4.5mW / °C above 70°C ambient temperature.

(Note 3) Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5,6,7 and 8 shorted together

(\*\*) 1.6mm below seating plane.

**Electrical Characteristics (unless otherwise specified,  $T_a = 0\sim 85^\circ\text{C}$ ,  $V_{CC} = 4.5\sim 20\text{V}$ ,  $I_{F(\text{ON})} = 1.6\sim 5\text{mA}$ ,  $I_{F(\text{OFF})} = 0\sim 0.1\text{mA}$ ,  $V_{EL} = 0\sim 0.8\text{V}$ ,  $V_{EH} = 2.0\sim 20\text{V}$ )**

Characteristic	Symbol	Test Condition		Min.	Typ.*	Max.	Unit
Output leakage current ( $V_O > V_{CC}$ )	$I_{OHH}$	$I_F = 5\text{mA}$ , $V_{CC} = 4.5\text{V}$	$V_O = 5.5\text{V}$	—	—	100	$\mu\text{A}$
			$V_O = 20\text{V}$	—	2	500	
Logic low output voltage	$V_{OL}$	$I_{OL} = 6.4\text{mA}$ (4 TTL load)		—	0.32	0.5	V
Logic high output voltage	$V_{OH}$	$I_{OH} = -2.6\text{mA}$		2.4	3.4	—	V
Logic low enable current	$I_{EL}$	$V_E = 0.4\text{V}$		—	-0.13	-0.32	mA
Logic high enable current	$I_{EH}$	$V_E = 2.7\text{V}$		—	—	20	$\mu\text{A}$
		$V_E = 5.5\text{V}$		—	—	100	
		$V_E = 20\text{V}$		—	0.01	250	
Logic low enable voltage	$V_{EL}$	—		—	—	0.8	V
Logic high enable voltage	$V_{EH}$	—		2.0	—	—	V
Logic low supply current	$I_{CCL}$	$I_F = 0\text{mA}$ $V_E = \text{don't care}$	$V_{CC} = 5.5\text{V}$	—	5	6.0	mA
			$V_{CC} = 20\text{V}$	—	5.6	7.5	
Logic high supply current	$I_{CCH}$	$I_F = 5\text{mA}$ $V_E = \text{don't care}$	$V_{CC} = 5.5\text{V}$	—	2.5	4.5	mA
			$V_{CC} = 20\text{V}$	—	2.8	6.0	
High impedance state output current	$I_{OZL}$	$I_F = 5\text{mA}$ $V_E = 2\text{V}$	$V_O = 0.4\text{V}$	—	1	-20	$\mu\text{A}$
			$V_O = 2.4\text{V}$	—	—	20	
	$I_{OZH}$	$I_F = 0\text{mA}$ $V_E = 2\text{V}$	$V_O = 5.5\text{V}$	—	—	100	
			$V_O = 20\text{V}$	—	0.01	500	
Logic low short circuit output current (Note 4)	$I_{OSL}$	$I_F = 0\text{mA}$	$V_O = V_{CC} = 5.5\text{V}$	25	55	—	mA
			$V_O = V_{CC} = 20\text{V}$	40	80	—	
Logic high short circuit output current (Note 4)	$I_{OSH}$	$I_F = 5\text{mA}$ $V_O = \text{GND}$	$V_{CC} = 5.5\text{V}$	-10	-25	—	mA
			$V_{CC} = 20\text{V}$	-25	-60	—	
Input current hysteresis	$I_{HYS}$	$V_{CC} = 5\text{V}$		—	0.05	—	mA
Input forward voltage	$V_F$	$I_F = 5\text{mA}$ , $T_a = 25^\circ\text{C}$		—	1.55	1.7	V
Temperature coefficient of forward voltage	$\Delta V_F / \Delta T_a$	$I_F = 5\text{mA}$		—	-2.0	—	mV / $^\circ\text{C}$
Input reverse breakdown voltage	$BV_R$	$I_R = 10\mu\text{A}$ , $T_a = 25^\circ\text{C}$		5	—	—	V
Input capacitance	$C_{IN}$	$V_F = 0\text{V}$ , $f = 1\text{MHz}$ , $T_a = 25^\circ\text{C}$		—	45	—	pF
Resistance (input-output)	$R_{I-O}$	$V_{I-O} = 500\text{V}$ R.H. $\leq 60\%$ (Note 3)		$5 \times 10^{10}$	$10^{14}$	—	$\Omega$
Capacitance (input-output)	$C_{I-O}$	$V_{I-O} = 0\text{V}$ , $f = 1\text{MHz}$ (Note 3)		—	0.6	—	pF

(\*\*) All typ. values are at  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $I_{F(\text{ON})} = 3\text{mA}$  unless otherwise specified.

## Switching Characteristics

(unless otherwise specified,  $T_a = 0\sim 85^\circ\text{C}$ ,  $V_{CC} = 4.5\sim 20\text{V}$ ,  $I_{F(\text{ON})} = 1.6\sim 5\text{mA}$ ,  $I_{F(\text{OFF})} = 0\sim 0.1\text{mA}$ )

Characteristic	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time to logic high output level (Note 5)	$t_{pLH}$	1	Without peaking capacitor $C_1$	—	235	—	ns
			With peaking capacitor $C_1$	—	—	400	
Propagation delay time to logic low output level (Note 5)	$t_{pHL}$		Without peaking capacitor $C_1$	—	250	—	ns
			With peaking capacitor $C_1$	—	—	400	
Output rise time (10–90%)	$t_r$			—	35	—	ns
Output fall time (90–10%)	$t_f$			—	20	—	ns
Output enable time to logic high	$t_{pZH}$	2	—	—	—	ns	
Output enable time to logic low	$t_{pZL}$		—	—	—	ns	
Output disable time from logic high	$t_{pHZ}$		—	—	—	ns	
Output disable time from logic low	$t_{pLZ}$		—	—	—	ns	
Common mode transient immunity at logic high output (Note 6)	$CM_H$	3	$I_F = 1.6\text{mA}$ , $V_{CM} = 50\text{V}$ , $T_a = 25^\circ\text{C}$	-1000	—	—	$\text{V} / \mu\text{s}$
Common mode transient immunity at logic low output (Note 6)	$CM_L$		$I_F = 0\text{mA}$ , $V_{CM} = 50\text{V}$ , $T_a = 25^\circ\text{C}$	1000	—	—	$\text{V} / \mu\text{s}$

(\*) All typ. values are at  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $I_{F(\text{ON})} = 3\text{mA}$  unless otherwise specified.

(Note 4) Duration of output short circuit time should not exceed 10ms.

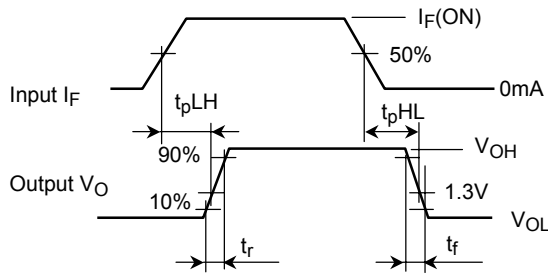
(Note 5) The  $t_{pLH}$  propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse.

The  $t_{pHL}$  propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.

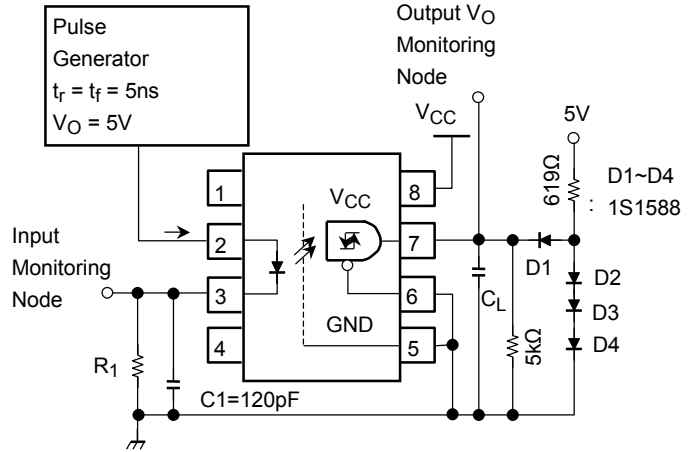
(Note 6)  $CM_L$  is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ( $V_O \leq 0.8\text{V}$ ).

$CM_H$  is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ( $V_O \leq 2.0\text{V}$ ).

**Test Circuit 1  $t_{pHL}$ ,  $t_{pLH}$ ,  $t_r$  and  $t_f$**

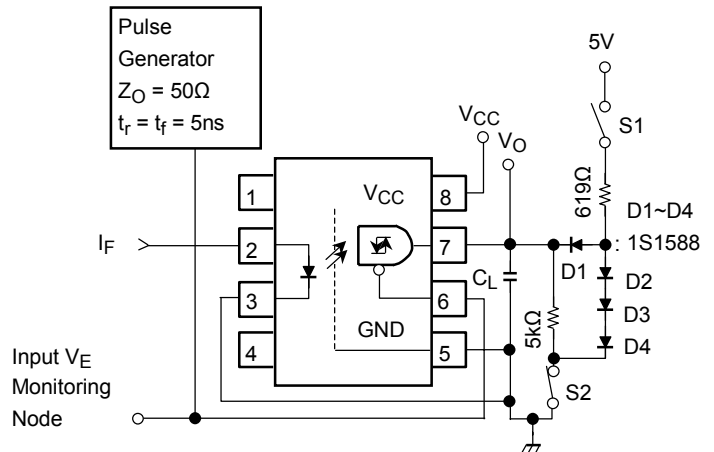
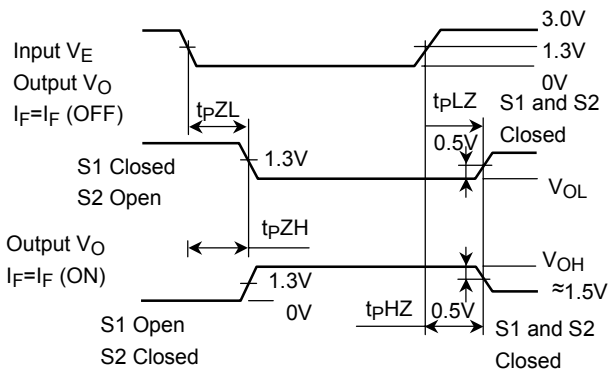


$R_1$	2.15k $\Omega$	1.1k $\Omega$	681 $\Omega$
$I_F(ON)$	1.6mA	3mA	5mA



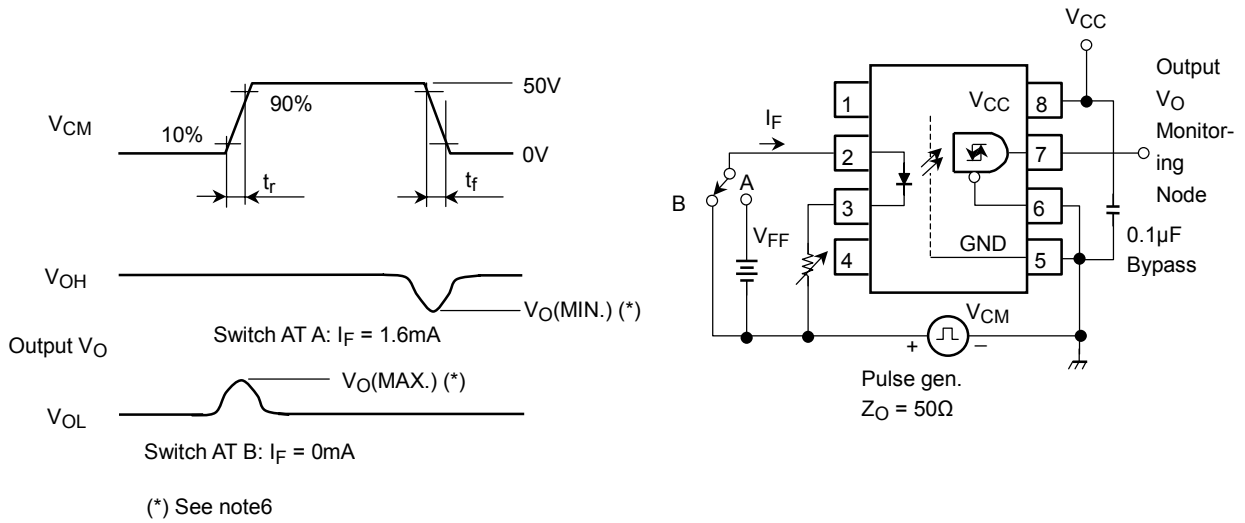
$C_1$  is peaking capacitor. The probe and jig capacitances are include in  $C_1$ .  
 $C_L$  is approximately 15pF which includes probe and stray wiring capacitance.

**Test Circuit 2  $t_{pHZ}$ ,  $t_{pZH}$ ,  $t_{pLZ}$  and  $t_{pZL}$**



$C_L$  is approximately 15pF which includes probe and stray wiring capacitance.

**Test Circuit 3 Common Mode Transient Immunity**



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